VLSI Interconnect Design Automation Using Quantitative and Symbolic Techniques

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Abstract— **This paper presents a framework for design automation of VLSI interconnect geometries. Crosstalk, overshoot, undershoot, signal delay, and line impedance are design performance parameters under consideration. Since the dependence of electrical performance parameters on geometry is not easily defined, both qualitative and quantitative techniques are used. Two knowledge bases are introduced—a model and simulation base. The model base contains models used for terminations, transmission line parameter extractors, and transmission lines. The simulation knowledge base contains a set of approximations and routines for the exact evaluation of electrical performance parameters. Procedures are introduced for the automatic extraction of applicable models and simulation techniques in the design process. An unconstrained optimization routine is used as a design search technique. The approach presented here gives faster results than approaches shown in literature, with little sacrifice of accuracy.**

Index Terms— **Interconnect design automation, model-based and simulation techniques, crosstalk, and signal delay optimization.**

I. Introduction

METHODS and tools for the automatic design of signal distribution have been addressed by few researchers. Dai [1] discusses a multichip module (MCM) router capable of changing the spacing and width of interconnects in order to meet crosstalk specifications. The limitation of his approach is the use of a lumped electrical model that does not facilitate design with respect to other geometrical parameters. Rainal [7] approximates interconnects as filaments. This approximation is inadequate for the design of cross-sectional geometry. Rather than using approximations for evaluation of crosstalk and other electrical performance parameters, Liu *et al.* [4] uses the inverse Laplace transform to compute the exact value for each electrical parameter. A min–max optimization method with a sensitivity analysis is used for the physical design of an interconnect. Min–max is a nonlinear, constrained, and multiple variable optimization method that can suffer from nonconvergence. It is also expensive computationally and requires numerous evaluations of electrical parameters of the circuit, each of which calls for inverse Laplace transform evaluation with a sensitivity calculation. We feel that the automation of interconnect design requires a combination of qualitative (symbolic) and quantitative (numerical) methods which should result in faster and more accurate design.

Conceptually, our approach to design automation is rooted in the notion of a search process through a space of design configurations. The design methodology is based on the following major steps: first, we select appropriate models for a given interconnect geometry. Then, we use simulators to evaluate a design state at hand. Optimization routines are then invoked and a new design state is produced. This process continues until no further improvements can be made to the interconnect design. We describe this process in detail in Section IV, where we present the design system.

Within our framework, we support two levels of geometric design. At the *design level*, the system attempts to meet the constraints but does not optimize line geometry with respect to the area. At the *optimization level*, the interconnect design is optimized with respect to both electrical and geometrical constraints.

Two knowledge bases are used to organize information about models and simulators used at each step in the design process. The *model base* contains models of terminations, transmission line parameter extractors, and the transmission lines. Models selected from the model base are used for the selection of an appropriate simulator at each design step. The *simulation base* contains both approximate and exact routines for the evaluation of electrical performance. Selection of models and simulators, setting up experiments for evaluation of electrical performance criteria, and running the optimization routine are controlled by a *design engine*. Examples shown in Section V illustrate both design and optimization levels for VLSI interconnect geometry design.

We now proceed to describe the major elements of our design approach and the realization of the resulting system for design of interconnect geometry with respect to electrical and area constraints. The electrical performance criteria considered are crosstalk, overshoot, undershoot, signal delay, and impedance. The transmission lines are assumed to be of identical geometry. They are terminated by either resistances or capacitances to represent either CMOS, BJT, or BiCMOS technologies. The configuration considered here has drivers at the near end and receivers at the far end of both the driven and quiet lines as shown in Fig. 1. The active line is driven by a step input voltage.

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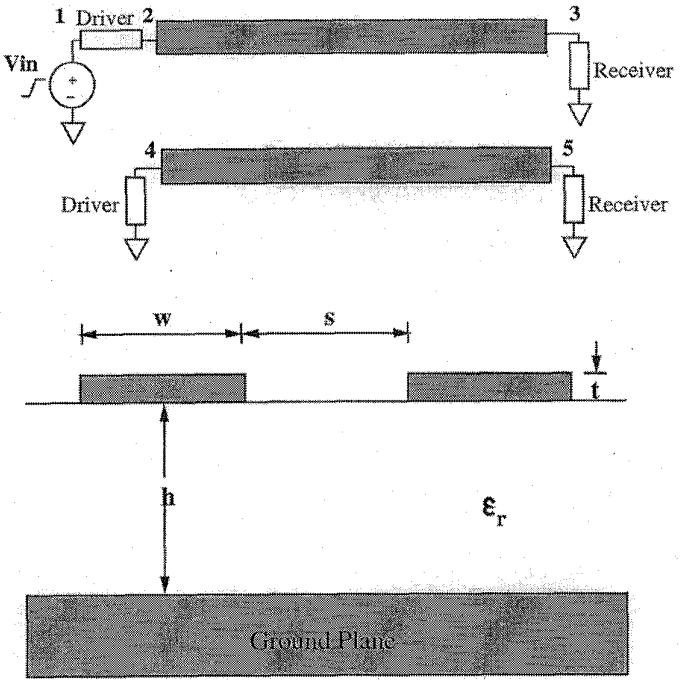

Fig. 1. Design configuration.

II. Model Base

Driver and receiver circuits are terminated by either CMOS or BJT components. CMOS technology is modeled by a voltage source connected in series with the resistor for a driver (R_d) and the capacitor as a receiver (C_l). Driver (R_d) and receiver resistances (R_l) are models for the BJT technology. A BiCMOS gate is modeled as a BJT terminated driver (R_d) and a CMOS-based receiver (C_l).

Two different techniques are used in this work to transform the geometrical parameters of the interconnect into electrical parameters: the approximate technique developed by Gupta [2] and the more exact University of Arizona Method of Moments TEM (UAMOM) transmission line extractor [10]. Both techniques give even and odd mode characteristic impedance and line delays, which are then used in either the lumped or the transmission line models. These two models are the basis of approximate methods for the evaluation of electrical performance criteria.

A. Lumped Line Model

The line is modeled by per unit length inductance L and capacitance C multiplied by the length of the line l. Kirchhoff's current and voltage laws are used to obtain a transfer function in the frequency domain for a resistive or a capacitive receiver. The driver voltage is assumed to be a step function. The line input voltage is limited by M and the transfer function of the lumped circuit

$$G(s) = \frac{\omega_0^2}{s^2 + 2\xi\omega_o s + \omega_0^2} \tag{1}$$

where M, ξ, and w_0 are defined depending on the type of terminations.

Resistive Termination:

$$4\xi^2 = \frac{\left(\frac{Ll}{R_l} + R_d Cl\right)^2}{\left(\frac{R_d}{R_l} + 1\right) LCl^2}$$

$$\omega_0^2 =, \frac{\frac{R_d}{R_l} + 1}{LCl^2}$$

$$M = \frac{Rl}{Rd + Rl}.$$

Capacitive Termination:

$$4\xi^2 = \frac{(C_l + Cl)R_d^2}{Ll}$$

$$\omega_0^2 = \frac{1}{(C_l + Cl)Ll}$$

$$M = 1. \tag{2}$$

The damping ratio, ξ, determines if the line response is overdamped ($\xi > 1$), under-damped ($\xi < 1$), or critically damped ($\xi = 1$). The natural frequency of response is determined by the value of ω_0.

An underdamped response results in overshoot and undershoot. If the line response is underdamped, the following equation results:

$$V_{out} = |V_{in}|M\left[1 - \frac{e^{-\xi\omega_0 t}}{\sqrt{1-\xi^2}} \sin\left(\omega_0 t\sqrt{1-\xi^2} + \theta\right)\right] \tag{3}$$

where

$$\theta = \arctan\frac{\sqrt{1-\xi^2}}{\xi}. \tag{4}$$

An overdamped response contributes to line delay. If the line response is overdamped, the following equation results:

$$V_{out} = |V_{in}|(1 - Ae^{-at} + Be^{-bt}) \tag{5}$$

where ξ and ω_0 are given in (2) and constants a, b, A, and B are defined as follows:

$$a = \xi\omega_0\left(1 - \sqrt{1 - \frac{1}{\xi^2}}\right)$$

$$b = \xi\omega_0\left(1 + \sqrt{1 - \frac{1}{\xi^2}}\right)$$

$$A = \frac{b}{b-a}$$

$$B = \frac{a}{b-a}. \tag{6}$$

B. Transmission Line Model

At higher operational frequencies or faster rise times, the lumped model is not adequate [12]. Thus, the transmission line analysis of coupled microstrips becomes a necessity. The exact time domain voltage and current responses of lossless transmission lines driven by a step input and terminated with either resistances or capacitances can be derived. Because the

far end response determines the operation of the system, this response is the focus of this paper. A similar derivation was done by Isaacs and Strakhov for lossy lines [3].

The transmission line equation in the frequency domain for voltage is

$$\frac{d_2}{dz^2}\begin{bmatrix}V_1\\V_2\end{bmatrix}=\begin{bmatrix}A_{11}, & A_{12}\\A_{21}, & A_{22}\end{bmatrix}\begin{bmatrix}V_1\\V_2\end{bmatrix} \tag{7}$$

where

$$\begin{aligned}A_{11}&=A_{22}\\&=-s^2(LC+L_mC_m)\end{aligned}$$

and

$$\begin{aligned}A_{12}&=A_{21}\\&=-s^2(LC_m+L_mC).\end{aligned}$$

When modal decomposition and inverse Laplace transform are applied, the exact response of driven (V_1) and quiet (V_2) lines at the far end results in

$$\begin{aligned}V_1&=V_+ + V_-\\V_2&=V_+ - V_-\end{aligned} \tag{8}$$

where V_+ and V_- are the even and odd mode voltages, respectively. For the capacitive receiver they are defined as follows:

$$\begin{aligned}&V_{(+,-)}\\&=K\sum_{n=0}^{\infty}K_n\sum_{m=0}^{n}K_m\\&\cdot\left\{1-\frac{e^{-a(t-b)}}{m!}\sum_{s=0}^{m}[a(t-b)]^{m-s}\prod_{p=0}^{s-1}(m-p)\right\}\end{aligned} \tag{9}$$

where b determines the delay of even and odd modes as they reflect at the far end for each trip $n=0, 1, \cdots$, a is the time constant required to charge up the load capacitance by the line, K is the driver injection coefficient, K_n is the driver reflection coefficient, and K_m is a constant. The values of the variables are

$$\begin{aligned}b&=\gamma_{(+,-)}l(2n+1)\\a&=\frac{1}{Z_{(+,-)}C_l}\\K&=\frac{V_{in}}{1+\dfrac{R_d}{Z_{(+,-)}}}\\K_n&=\left[\frac{Z_{(+,-)}-R_d}{Z_{(+,-)}+R_d}\right]^n\\K_m&=(-2)^m\frac{n!}{(n-m)!m!}.\end{aligned} \tag{10}$$

For the resistive receiver, even and odd mode voltage definitions are

$$V_{(+,-)}=K\sum_{n=0}^{\infty}(\Gamma_d\Gamma_l)^n u[t-b] \tag{11}$$

where b determines the delay of even and odd modes as they reflect at the far end for each trip $n=0, 1, \cdots$, Γ_d and Γ_l are the driver and the receiver reflection coefficients, respectively, and K is the driver and load injection coefficient. They are determined as follows:

$$\begin{aligned}b&=\gamma_{(+,-)}l(2n+1)\\\Gamma_d&=\frac{[R_d-Z_{(+,-)}]}{[R_d+Z_{(+,-)}]}\\\Gamma_l&=\frac{[R_l-Z_{(+,-)}]}{[R_l+Z_{(+,-)}]}\\K&=\frac{V_{in}}{\left[1+\dfrac{R_d}{Z_{(+,-)}}\right]\left[1+\dfrac{Z_{(+,-)}}{R_l}\right]}.\end{aligned} \tag{12}$$

C. Model Rulebase

The model rulebase consists of two parts—rules for the selection of an appropriate parameters extractor and rules for the selection of models used in simulation. Each rule consists of two parts—a premise (or the "if" part) and the conclusion (or the "then" part). When the premise is satisfied, the selection specified in the conclusion is made.

The condition for the selection of Gupta's model for the even and odd mode characteristic impedances and delays was established by computing predictions using the UAMOM program [10]. Gupta's model for both impedances and delays was found to be within 10% of UAMOM's values for the following conditions:

$$\begin{aligned}0.01&\le\frac{s}{h}\\&\le 10\\0.01&\le\frac{w}{h}\\&\le 10\\\epsilon_r&\ge 1\\\frac{s}{t}&>2.\end{aligned} \tag{13}$$

The rule for the selection of Gupta's model is

```
if      (Gupta'a condition is satisfied)
then    (select Gupta's model).
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If (13) is not satisfied, UAMOM is selected. The chosen extractor serves to transform the geometrical parameters of the interconnects into the corresponding electrical parameters.

At this point, the selection of a lumped or a transmission line model is made. The choice depends upon how the electrical performance parameters are to be evaluated. Two methods are used—exact and approximate. If the exact evaluation techniques are to be used, then the transmission line model is always selected. Thus, rules are needed only when the approximated performance evaluation is carried out. The rules deciding which approximate transmission line model should be used are based on dimensionless parameters of the driver, receiver, and interconnect system. Electrical parameters, L, C,

L_m, C_m, R_d, R_l, and C_l, are transformed into dimensionless parameters using the equations

$$r_d = \frac{R_d}{Z_0}$$
$$r_l = \frac{R_l}{Z_0}$$
$$c_l = \frac{C_l}{Cl}$$
$$k_l = \frac{L_m}{L}$$
$$k_c = \frac{-C_m}{C}. \tag{14}$$

When the transformation is performed, both the lumped and transmission line response can be represented as a function of only dimensionless parameters together with the characteristic impedance of the line Z_0 and the line delay T_d. Simulations were performed to determine where the truncated transmission line model was more applicable than the lumped line model, for the range $0.01 \Leftarrow c_l$, $r_d \Leftarrow 100$. The lumped and the truncated transmission line models [$n = 1$ in (9)] were compared with the exact values of far end voltages as given by (9). The tests to determine applicable models were performed not only for different values of terminations, but also for different values of coupling coefficients k_l and k_c. We determined that the selection rules are functions of terminations only.

The *capacitive condition* is defined as [($c_l < 0.1$) and ($r_d < 1.0$)]. When it is satisfied, the truncated transmission line model is selected with less than 10% error. Otherwise, the lumped model is used.

When the *resistive condition* [($r_d > 0.1$) and ($0.1 < r_l r_d < 10$)] is satisfied, the truncated transmission line model is within 10%. The lumped model is more accurate than the truncated transmission line model outside this range. Simulation shows that a quiet line is for all cases described within 10% by the truncated transmission line model.

III. Simulation Base

The simulation knowledge base contains both exact and approximate techniques for the evaluation of electrical performance parameters. It is overlayed with a rulebase capable of choosing the best technique for a given set of terminations and the selected transmission line model.

Two sets of approximations are presented for the evaluation of overshoot, undershoot, signal delay, and crosstalk. They are based on the lumped and transmission line models. This is followed by the description of the exact and filtered routines which are used to obtain values for electrical performance criteria. Although not a performance parameter itself, the characteristic impedance of the line is added to the electrical performance criteria to allow the designer to indirectly control other constraints, e.g., switching noise [12]. Impedance is calculated directly from the extracted parameters of the line, i.e., $Z = \sqrt{L/C}$.

A. Approximate Evaluation of Performance Criteria Using Lumped Model

When terminations are not matched with the transmission line, overshoot occurs due to reflections of the signal at the terminations. High overshoot causes higher power consumption and degrades the reliability of the receivers but does not cause them to switch falsely. The overshoot calculation is the same for both the resistive and capacitive terminations. The definition of the damping parameter, ξ, is given in (2)

$$\text{Overshoot} = V_{\text{in}}\left[1 + e^{-(\pi\xi)/\sqrt{1-\xi^2}}\right]. \tag{15}$$

Undershoot and overshoot are related to each other—typically the highest value of overshoot is followed by the lowest value of undershoot. Undershoot can cause false switching at the receiver end if it is large enough and lasts long enough for the receiver to switch

$$\text{Undershoot} = V_{\text{in}}\left[1 + e^{-(2\pi\xi)/\sqrt{1-\xi^2}}\right]. \tag{16}$$

Signal delay slows down the response of the entire system. It is calculated by simulating either the overdamped (3) or underdamped (5) response of the lines until the time when $V_{\text{far}}/V_{\text{in}} > 0.5$ (or other user-defined ratio). This time is then noted as the signal delay.

Crosstalk is caused by electromagnetic coupling between transmissions lines in proximity of each other. When a lumped model is selected for calculations, then different equations are used depending on whether the even and odd mode damping coefficients show underdamped (5) or overdamped (3) response. Crosstalk is the difference between the even and odd mode lumped approximations

$$\text{Crosstalk} = V_+ - V_-. \tag{17}$$

B. Approximate Evaluation of Performance Criteria Using Transmission Line Model

The maximum value of overshoot that might be registered by the receiver occurs when the even mode voltage arrives at the far end and lasts until the first reflection of the odd mode arrives at the far end. Thus, a way to approximate overshoot is to take the first two terms in the far end voltage response of the driven line from the exact solution and to evaluate the overshoot in the middle of the interval. All constants are defined in (10)

$$\text{Overshoot} = K_+[1 - e^{-a_+(2T-b_+)}] + K_-[1 - e^{-a_-(2T-b_-)}]. \tag{18}$$

In the case of resistive termination, the following equations can be used to estimate the overshoot. Equation (12) contains the definition of all constants

$$\text{Overshoot} = K_+ + K_-. \tag{19}$$

The maximum value of undershoot occurs when the first reflection of the even mode off the near end comes to the far end and lasts until the second reflection of the odd mode arrives at the far end of the line. Thus, a way to approximate undershoot is to take the first four terms from the exact solution

of the far end voltage response of the driven line and evaluate undershoot in the middle of the time interval that it takes for the second reflection to arrive. Values of constants are given in (10). For the capacitive termination, undershoot is calculated as follows:

$$\begin{aligned}\text{Undershoot} = {} & K_+[1-e^{-a_+(4T-b_+)}]+K_-[1-e^{-a_-(4T-b_-)}] \\ & -K_-[1-e^{-a_-(4T-3b_-)}]\Gamma_-[2a_-(4T-3b_-)+1] \\ & -K_+[1-e^{-a_+(4T-3b_+)}]\Gamma_+[2a_+(4T-3b_+)+1]. \quad (20)\end{aligned}$$

For the resistive termination, the following equation applies:

$$\text{Undershoot} = K_- + K_+ + K_-\Gamma_{l-}\Gamma_{d-} + K_+\Gamma_{l+}\Gamma_{d+}. \quad (21)$$

The transmission line model is used to calculate the delay when the signal delay is between the odd and even mode delays. Again, signal delay is the time it takes for the voltage response at the far end to reach 50% of its maximum value [the constants are defined in (10)]

$$V_{\text{out}} = K_+[1-e^{-a_+(t-b_+)}]+K_-[1-e^{-a_-(t-b_-)}]. \quad (22)$$

Usually the maximum value of crosstalk that can be registered at the receiver occurs between the first incidence of the even mode and the arrival of the first reflection of the odd mode. The crosstalk is evaluated in the middle of this time interval. This approximation is derived by using the first two terms in the exact response. For a capacitive receiver, the following approximation is used [the constants are defined in (10)]:

$$\begin{aligned}\text{Crosstalk} = {} & K_+[1-e^{-a_+(2T-b_+)}] \\ & -K_-[1-e^{-a_-(2T-b_-)}]. \quad (23)\end{aligned}$$

If the receiver is resistive, then the following approximation applies [constants are defined in (12)]:

$$\text{Crosstalk} = K_+ - K_-. \quad (24)$$

C. Evaluation of Electrical Parameters Using the Exact Routine

The exact routine uses (9) and (11) for the evaluation of far end voltages at the active and quiet lines. At low values of load capacitance, spikes appear at the output. The designer can chose to use either a low-pass filter or the exact response for the evaluation of electrical performance parameters depending on the sensitivity of the receiver to the spikes. The cut-off frequency for the filter is specified by the designer.

For both the exact and filtered responses, the maximum value of the voltage at the receiver on the driven line is taken as the measure of overshoot. The measure of crosstalk is taken to be the maximum voltage at the far end of the quiet line. The measure of undershoot is calculated as the minimum value of voltage at the far end of the driven line in the time interval after overshoot has been registered. The measure of delay is calculated by noting the time it takes for the far end voltage response on the driven line to reach a user-defined percentage of the amplitude of input voltage.

D. Simulation Rulebase

The premise of a simulation rule consists of the choice of the line model and the receiver models, which are given in the conclusion of the model rulebase. The conclusion of the simulation rulebase gives the name of an appropriate technique for the evaluation of a given electrical parameter. For example, a rule that would select an appropriate approximation of overshoot for which a lumped line model was selected for the capacitive receiver has the following form:

```
if   (lumped model is selected and
      the receiver is capacitive)
then
     (use overshoot approximation that utilizes
     the lumped line model and
     the capacitive receiver model).
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Similar rules have been developed for all the approximation techniques. When approximations show that design is satisfactory with respect to the electrical performance criteria specified by the user, the exact routines with filtered response are used to fine-tune the design.

IV. Design System

The overall configuration of our design system is shown in Fig. 2. Both the qualitative and quantitative approach are integrated within this system. In the qualitative phase of the design process, a set of model names for the selection of a simulator is generated. The quantitative phase results in a set of measures reflecting the performance characteristics of the current design. An optimization routine is invoked that generates the optimal value of the geometrical dimensions under consideration, e.g., the spacing which best meets the crosstalk requirements.

Models used in the system were described in Section II, together with rules to select an appropriate model at each design stage. The various models which are available imply different approximation techniques. The simulation base contains the information about tools used for performance evaluation. Each approximation is valid only for a specific set of models as discussed in Section III.

Our design engine controls the design process. It selects the appropriate models for a given interconnect geometry. Then, simulators are used to evaluate the current design state. The result of this stage is a set of values of performance parameters. The function to be minimized during the optimization phase is then formulated by the design engine. Finally, the optimization routine is invoked; this results in the next design state. This process continues until a satisfactory design is produced.

More details about the components of the design system are given in the ensuing sections. First the organization of knowledge in model and simulation bases is shown. Then, we discuss how the selection of appropriate models and simulators is made. This is followed by a brief description of the design engine's tasks. Examples are given to demonstrate the efficacy of our approach.

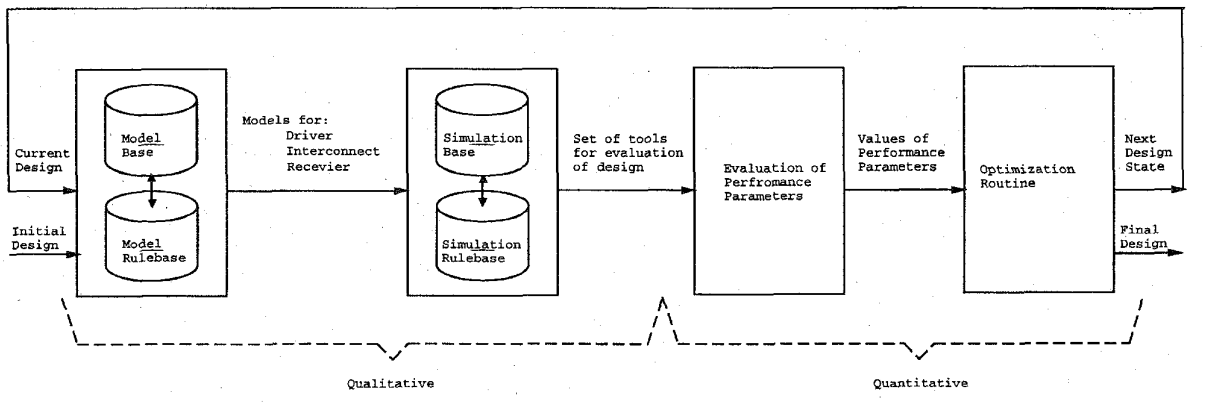


Fig. 2. Design system configuration.

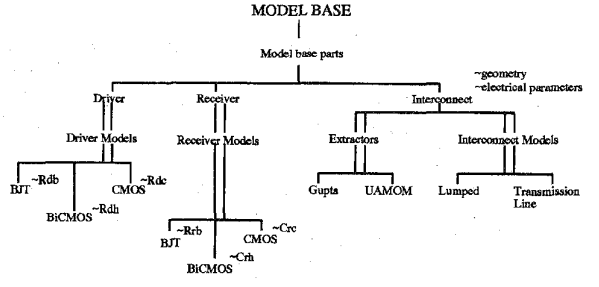


Fig. 3. SES of the model base.

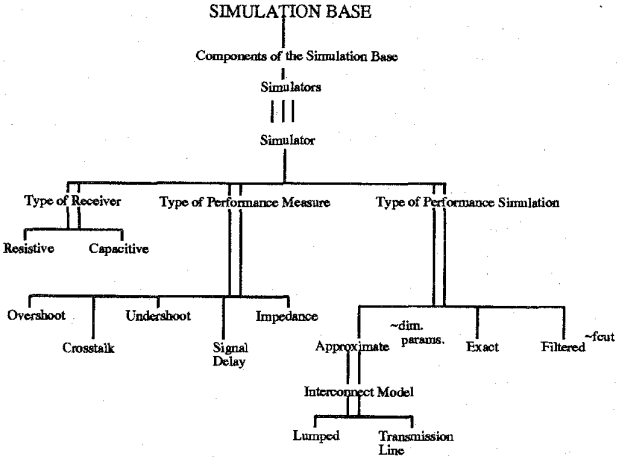


Fig. 4. SES of simulation base.

A. Model and Simulation Base Organization

The multiplicity of models and tools which can be used for the evaluation of electrical performance criteria requires a scheme for organizing and managing knowledge needed to select an adequate model and simulation tool.

The knowledge in the model and simulation bases is organized and managed using the system entity structure (SES) representation scheme (for details we refer the reader to [8]). SES facilitates a hierarchical and modular representation of domain knowledge.

It is a tree-like structure whose nodes can be: 1) entities, i.e., objects that represent part of the system being designed, e.g., a system component or a process; 2) aspects, i.e., modes of decomposing entities into its subcomponents; 3) specializations, i.e., a means of expressing taxonomic relationships among entities; and 4) attributes of entities. The entity nodes have to alternate with aspects and specializations; graphically (|) represents aspects, (||) represents specializations, and (~) is for attributes that characterize an entity. More information about SES and illustrative examples from the VLSI interconnect design domain are given in [8]. Here, we employ the SES as an underlying representation to organize and manage the model and simulation bases of our design system.

Fig. 3 shows the SES for the model base. Entities are objects of the design domain, for example, "driver" in the model base aspect of the "model base." As stated above, specialization is a mode of classifying an entity. For example, BJT, BiCMOS, and CMOS, are specifications of a driver in the driver model type specialization. There are two ways of specializing interconnect—one with respect to model used and the other with respect to the extractor, which is applied to obtain electrical parameters of transmission lines geometry.

The attributes characterize static and dynamic properties of an entity. For example, attributes of different driver and receiver technologies are the appropriate resistances and capacitances.

The system entity structure of the simulation base is shown in Fig. 4. It organizes knowledge about the simulation tools to be used for evaluation of design.

B. Rulebase

The system entity structure underlies a combinatorially unfolding number of alternative system designs, depending on the aspects and specializations selected. Rule-based pruning derives a structure called a design *composition tree* [9]. In the composition tree, unique model instances are associated with leaf components. An internal node of the tree is a coupling of the models associated with the internal node's children. A sample composition tree for the model base is given in Fig. 5.

A sample simulation composition tree is shown in Fig. 6. It was derived using the model composition tree shown in Fig. 5. The components of the model base composition tree

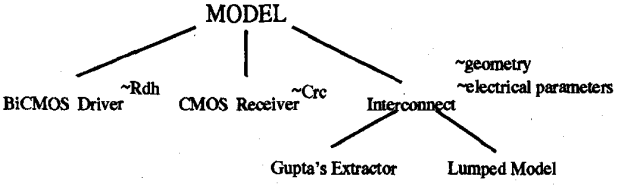


Fig. 5. A sample composition tree of the model base.

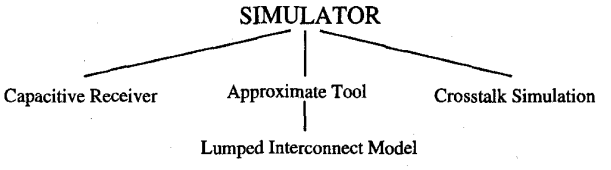


Fig. 6. A sample composition tree of the simulation base.

drive the selection of the approximate simulation techniques in the simulation SES.

C. Design Engine

The design engine controls the entire design process. The process can be viewed as a traversal of the design state space in a manner that produces the final design from the starting configuration. In our approach to interconnect design, the starting configuration is the initial interconnect geometry. A search is needed to provide a new set of geometrical parameters that the meet user's constraints. The parameters are: spacing, width, thickness, height, and the dielectric constant.

For each geometrical parameter, search is carried out to obtain an optimal design. The design engine takes the current geometry (state of design) and applies it to the model base as illustrated in Fig. 7. A model composition tree is generated based on the underlying SES. Next, the composition tree is used together with the user's choices of performance variables and the type of simulator to define a set of simulation composition trees. This is accomplished by successively performing a search through the simulation base SES. Once a set of simulation tools is chosen, the design engine forms a module called an *experimental frame* for the evaluation of the performance variables.

An experimental frame is a set of circumstances under which a model is experimented with and observed [13]. It is a means of instrumenting the model with a specification necessary for the execution of a simulation run.

In our framework, a simulation tool selected by the design engine is instrumented by an experimental frame in order to compute the values of electrical performance variables. The results of a simulation for all of the selected performance parameters are combined to form a function used in the optimization phase. The optimization routine is invoked by the design engine to generate the next design state. This process is repeated until a satisfactory design is generated.

D. Optimization

The design engine chooses appropriate models and simulation tools and forms the design objective function. Since none

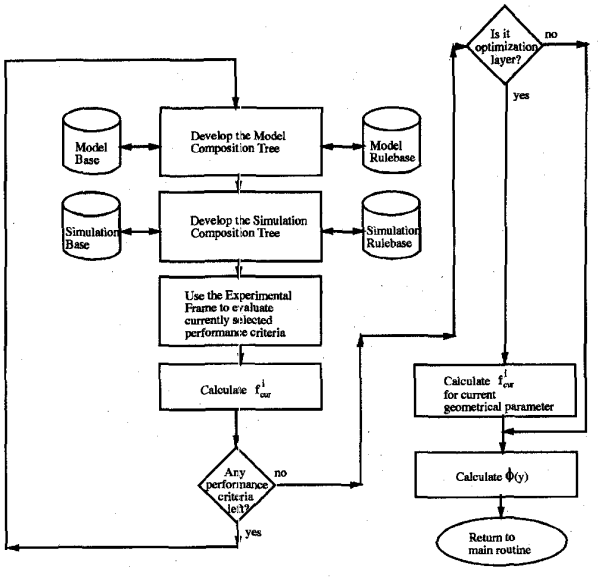


Fig. 7. Design system flow chart.

of the electrical performance parameters exhibit a behavior that is easy to characterize in terms of symbolic rules with respect to geometrical parameters, an algorithmic method is needed to find the amount by which any one of the geometrical parameters needs to be changed to optimize the objective function. The method selected in this work optimizes one geometrical parameter at a time with respect to any combination of electrical performance criteria chosen by the designer. This method was selected because it is faster, but it does limit the design space. The simulations run did not show a need for a more complex method at this time, although the extension of this system to include the more general optimization method is quite simple—only the optimization routine would have to be replaced.

Because each of the geometrical parameters is constrained, we use a simple transformation sufficient to convert the constrained design problem to an unconstrained one [5]. In the transformation given below, y is the unconstrained variable which is used in the optimization routine and x (any one of the geometrical parameters) is limited to $[x_L, x_U]$

$$x = x_L + (x_U - x_L) \sin^2 y. \tag{25}$$

Performance measures, f^i, are defined for each of the electrical performance parameters. Of all of the functions f^i, one which currently has the maximum value is minimized. Thus, the design objective function is defined as follows:

$$\psi = \min \{\max [f^i(y)]\}. \tag{26}$$

The variable i signifies any one of the five electrical performance parameters or, if the optimization layer is selected, a currently designed geometrical parameter. The constant y stands for the current unconstrained geometrical parameter used in design. [The definition of $f^i(y)$ is shown in (27).]

Overshoot, undershoot, crosstalk, and signal delay are all to be minimized. The performance measures which are used for the configuration of the design objective function for each

TABLE I
INITIAL GEOMETRY USED FOR ALL EXAMPLES IN SECTION V

Geometrical Parameters	Value	Unit	Electrical Parameters	Value	Unit
Line Length	10	cm	Line Inductance (L)	4.97	nH/cm
Spacing	4	–	Line Capacitance (C)	0.265	pF/cm
Height	10	–	Coupline Inductance (Lc)	1.87	nH/cm
Width	5	–	Couplig Capacitance (Cc)	0.105	pF/cm
Thickness	1	–	Characteristic Impedance (Zo)	67	Ω
Dielectric Constant	9.3	–	Line Delay (Td)	0.363	ns

of them is defined below. Functions f^i_{cur}, $f^i_{\max}$, and $f^i_{\min}$ are the current, maximum, and minimum value of performance parameters, respectively

$$f^i(y) = \frac{f^i_{\text{cur}} - f^i_{\max}}{f^i_{\max}}. \tag{27}$$

The design for impedance needs to be constrained between its minimum and maximum values. Thus, two measures are needed to define the design objective function for impedance. One is for minimization, as shown in (27). The other is for maximization. The maximization function is defined by

$$f^i(y) = \frac{f^i_{\min} - f^i_{\text{cur}}}{f^i_{\max}}. \tag{28}$$

The optimization layer adds another parameter to the optimization function. If the user desires to decrease a currently selected parameter in design, then the minimization function given in (27) is used. Otherwise, the maximization function is used as given in (28).

Once the function to be optimized is defined, a standard unconstrained optimization routine is used. A variety of unconstrained optimization routines can be chosen, depending on whether a derivative of the function being minimized is available or not. Since, in our case, it is not possible to compute a derivative by any other means than a numerical estimation (which is highly prone to error), we decided to use Brent's method [6]. It does not require derivative information and is known to converge to a solution superlinearly.

V. EXAMPLES

Section IV presented a system for the design of the interconnect geometry of two coupled microstrip lines with respect to electrical and geometrical performance criteria. This section gives examples of the design and optimization layers of our system. In each level, spacing is designed to meet crosstalk requirements for both the resistive and capacitive receivers. The tradeoff between crosstalk and spacing is selected since it is well known that as spacing is increased, crosstalk decreases. Both specific and a generic design examples are given which illustrate the capabilities of the design system.

A. Design Level

The parameters used in the design and optimization layers for the reduction of crosstalk are shown in Table I. Both capacitive and resistive receivers are used. In both cases, spacing is restricted to be between 2–8 and the driver resistance is set to 100 Ω. Notice that all parameters except for line length are unitless since it is their ratio, not the absolute value, that is important.

In the case of a capacitive receiver, the maximum value of crosstalk is set to 0.5 V. The load capacitance is 0.1 pF. The information presented above is given by the designer in the initialization phase of design.

Specification of driver and receiver circuits partially prunes the model base system entity structure shown in Fig. 3. The only choice left to the design engine is the selection of the interconnect model and the extractor. The designer's selection of the approximated type of performance simulation, crosstalk as a type of performance measure, and the capacitive receiver partially prunes the system entity structure of the simulation base shown in Fig. 4.

When the design system is invoked, the design engine first makes a selection of the extractor to be used to obtain electrical parameters of the current geometry. For geometry parameters given in Table I, Gupta's extractor is selected as shown by the condition of (13). Extraction is performed next. The output of extraction gives electrical parameters of the line which can then be transformed together with terminations into dimensionless parameters shown in (14).

Then, an appropriate interconnect model is selected. For values of terminations given by the designer and electrical parameters of line shown in Table I, a lumped model is selected. This completes the specification of the model composition tree. The final configuration is shown in Fig. 5. The model composition tree is used to complete the simulation composition tree. Names of models selected by the design engine are used as premises in selection rules in the simulation base. The simulation composition tree is shown in Fig. 6. It uniquely identifies the name of the procedure to be used for evaluation of crosstalk.

Next, the design engine formulates the simulation run specification. The maximum value of voltage needed by the generator and the time to end simulation are both specified by the designer in the initialization part of the system. This information is sufficient for crosstalk evaluation. When a value of crosstalk is obtained, the design objective function is formulated. Since crosstalk is the only performance criterion selected, and it is to be minimized, the value of $f^i(y)$ for crosstalk is calculated using (27). Variable y is the current value of spacing transformed into its unconstrained version as given by (25). The value of the design objective function ϕ is the maximum of individual f^i's. In this case, it is the value of performance measure of crosstalk, $f^i(y)$, since there

TABLE II
RESULTS FOR DESIGN AND OPTIMIZATION OF SPACING WITH RESPECT TO CROSSTALK

				Spacing ($2 < s < 8$)	Crosstalk			
Case	Level	R_d	Z_l	final value	limit	approx.	exact	error
1	Design	100 Ω	0.1 pF	8	0.5 V	0.436 V	0.435 V	0.2%
	Optim.	100 Ω	0.1 pF	6.9		0.496 V	0.504 V	1.6%
2	Design	100 Ω	100 Ω	8	0.15 V	0.102 V	0.103 V	0.1%
	Optim.	100 Ω	100 Ω	5.5		0.146 V	0.143 V	2.1%

are no other performance criteria. This value is forwarded to the optimization routine which then attempts to find the value for spacing that minimizes the design objective function. At each evaluation of the design objective function, the entire process of deriving model and simulation composition trees, evaluating performance criteria, and finally of obtaining the value for the design objective function is repeated. The same process is applied for the optimization layer, except that the criteria which reflect the desired direction of change for the current geometrical parameter are added to the design objective function as discussed in Section IV. This design process continues until a geometry which meets all of the performance criteria is obtained.

Results of our design are summarized in Table II. The design engine chose the largest value of spacing as optimum at design level because the tradeoff between area and crosstalk was not included.

To compare the value of crosstalk obtained using approximations with the exact value, an exact simulation is done. Section II contains equations which are used by the exact routine. As can be seen in Table II, the approximation (0.436 V) is very close to the exact value of crosstalk (0.435 V). In fact, in any realistic case the load capacitance is much lower than line capacitance and driver resistance is on the order of line impedance. Whenever this is true, the approximations give results that are within 10% of the exact value.

Similar results are obtained with resistive receiver. Resistance is set to 100 Ω. The maximum allowable value of crosstalk is set to 0.15 V. Again, the design engine chose the maximum value of spacing. The value of crosstalk for maximum spacing is well below the maximum allowed. The error between crosstalk approximation and the exact value is only 0.1%.

B. Optimization Level

The design produced by the design level is now optimized with respect to spacing. Typically, a designer wants to conserve area while keeping crosstalk at a reasonable level. Thus, the preferred direction of change for spacing is to decrease it. This level attempts to find the minimum spacing that still satisfies the crosstalk constraint. All of the other variables are the same as in the design level and are given in Table II.

In the case of the capacitive receiver, the best value of spacing given by optimization level is 6.9. At this value of spacing crosstalk is approximated to be 0.496 V, which is right below the 0.5 V maximum specified by the designer. Again, simulation is done to check if the approximated value of crosstalk is correct. The value of crosstalk given by the exact routine is 0.504 V, which is basically the same as approximation—only 1.6% error. Results of optimization are summarized in Table II.

When a resistive receiver is used, the best value of spacing chosen by optimization level is 5.5. Again, the approximation (0.146 V) is right below the maximum allowed value (0.15 V). The exact value is 0.143 V, which gives a 2.1% error.

It is clear from these examples that the system is capable of designing an interconnect geometry that meets all electrical criteria specified by the designer. More general designs have been done with equally good results [11]. The design process takes only a few seconds on a Sun Sparc II workstation. If the exact simulator was used, or a general simulator such as Spice, the time needed to finish the design would rise by couple orders of magnitude with practically no advantage in accuracy. The approach presented by Liu *et al.* [4] takes on the average 1.5 h, as compared to 6 s required by the tool presented here. Geometries which result from this design compare well with geometries shown in the literature, i.e., in [7] and [12]. As a result, combining qualitative and quantitative approaches is better than using only a quantitative approach as has been done up to now in package design.

VI. CONCLUSION

This paper presented an automation approach and tools for design of interconnect geometry with respect to electrical and area constraints. The electrical performance criteria considered are crosstalk, overshoot, undershoot, signal delay, and impedance. Although not a performance parameters itself, the characteristic impedance of the line is added to the electrical performance criteria to allow the designer to indirectly control other constraints such as switching noise.

The advantage of combining the symbolic and quantitative approaches is in the separation of design knowledge from the procedures which manipulate it. New knowledge can be easily added and used in other designs.

An algorithmic approach was necessary for optimization since the knowledge-based approach is not capable of handling that problem. Also, an algorithmic approach is needed for simulation, which is used for design evaluation. If only an algorithmic approach was used, the design would take a lot longer (1.5 h). Application of knowledge reduces the design space and thus reduces the complexity of the design problem. As more knowledge is added to the program and as better approximations are included, the design becomes better and faster.

Future work should consider the following areas: modifications to the model base, the simulation base, and additions of new performance criteria.

New models can be easily added to model base, since its organization is hierarchical and modular. So far, only the lossless line model was considered. The same methodology could be applied to design of a lossy line geometry. A lossy line model would be added to the model base SES and a rule which selects lossy versus lossless line model would augment the rule base. In addition to that, the tools for the evaluation of electrical performance criteria for lossy lines and their respective rules would populate the simulation base system entity structure. In this way, on-chip RC lines could be designed as well.

Similarly, to extend this design methodology to the three line case, appropriate models need to be added to model and simulation bases which allow for evaluation of electrical performance criteria in case of three lines. The rest of the system would stay unchanged.

Another area of improvement is to develop better models for driver and receiver circuits. Again, this would require only changes to model base and simulation base.

So far, the simulators in the simulation base were restricted to a step input. In reality, there is always a finite rise time, thus an improved design methodology should consider the effects of rise time on interconnect and termination design.

This work treated dielectric constant as a continuous parameter, which of course is not true in reality. This restriction can be easily removed by allowing user's to specify a table of allowed dielectric constants and then choose the nearest value to the one obtained through unconstrained optimization.

Finally, additional performance criteria need to be added to make design more realistic. Package design contains many other constraints which were not considered in this work, i.e., design of power and ground planes to reduce switching noise, and thermal constraints. The long-term goal of this project is to develop a package compiler which would aid in design of packages with respect to constraints on all levels of abstraction. The program for automation of interconnect design is only a stepping stone toward this goal.

REFERENCES

[1] W. W. Dai, "Performance driven layout of thin-film substrates for multichip modules," *Int. J. High Speed Elec.*, vol. 2, pp. 114–121, Nov. 1991.

[2] K. C. Gupta, R. Garg, and I. J. Bahl, *Microstrip Lines and Slotlines.* Norwood, MA: Artech, 1979, ch. 8.

[3] J. C. Isaacs and N. A. Strakhov, "Crosstalk in uniformly coupled LOSBY transmission lines," *Bell System Tech. J.*, vol. 52, no. 1, pp. 101–115, Jan. 1973.

[4] R. Liu, Q. Zhang, and M. Nakhla, "A frequency domain approach to performance optimization of high-speed VLSI interconnects," *IEEE Trans. Comp., Packag., Manufact. Technol.*, vol. 40, no. 12, pp. 2403–2411, Dec. 1992.

[5] R. E. Massara, *Optimization Methods in Electronic Circuit Design.* New York: Harlow Longman Scientific Publishing, 1991.

[6] W. Preas, B. Flannery, S. Teukolsky, and W. Vetterling, *Numerical Recipes in C.* Cambridge: Cambridge Univ. Press, 1988.

[7] A. J. Rainal, "Transmission properties of balanced interconnections," *IEEE Trans. Comp., Hybrids, Manufact. Technol.*, vol. 16, no. 1, pp. 137–145, Feb. 1993.

[8] J. W. Rozenblit and J. Hu, "Integrated knowledge representation and management in simulation-based design generation," *Math. Comput. Simulation*, vol. 34, pp. 261–282, 1992.

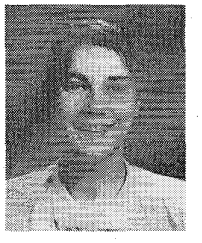
[9] J. W. Rozenblit and Y. M. Huang, "Rule-based generation of model structures in multifaceted modeling and system design," *ORSA J. Computing*, vol. 3, no. 4, pp. 330–344, Fall 1991.

[10] M. R. Scheinfein, "Method of moments TEM transmission line parameter calculator theory of operation and user's guide," M.S. thesis, Univ. of Arizona, June 1986.

[11] T. Simunic, "VLSI interconnnect design using qualitative and quantitative techniques," M.S. thesis, Univ. of Arizona, Dec. 1993.

[12] R. R. Tummala and E. J. Rymaszewski, Eds., *Microelectronic Packaging Handbook.* New York: Van Nostrand Reinhold, 1989.

[13] B. P. Zeigler, *Theory of Modeling and Simulation.* New York: Wiley, 1976.



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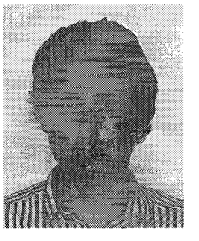

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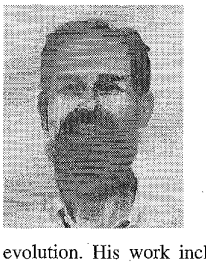

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